

CS8421-10-30-2006

Instruction Sets & CPU Design

CS8421

Computing Systems

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Class

Will

Start

Momentarily...

We need to develop an instruction set and formats that support the following operations:

$R1 \leftarrow R1 \text{ OP } R2$, 64 instructions

$R3 \leftarrow R1 \text{ OP } R2$, 64 instructions

$\text{MEM} \leftarrow R1$, 64 instructions

$\text{MEM} \leftarrow R1 \text{ OP } R2$, 32 instructions

$R3 \leftarrow R1 \text{ OP } \text{MEM}$, 32 instructions

The machine has 16 general purpose registers, each 16 bits in size. Memory is accessed by a base plus displacement of 8 bits.

R1 ← R1 OP R2

R1 ← R2 OP R3

MEM ← R1

MEM ← R1 OP R2

R1 ← R2 OP MEM

OP R1 R2

OP R1 R2 R3

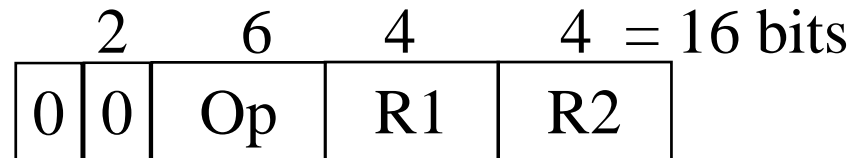
OP R1 B2 D2

OP R1 R2 B3 D3

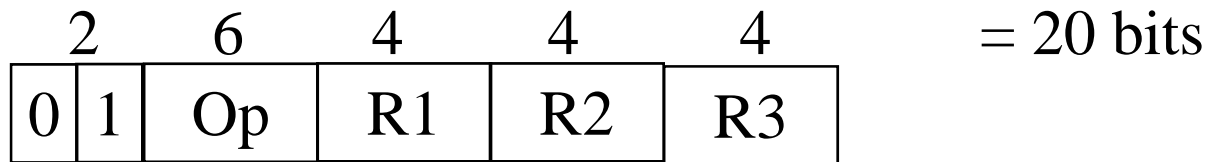
OP R1 R2 B3 D3

4 Formats needed, two bits for the format specification. 64 instructions in each format (6 bit opcode)

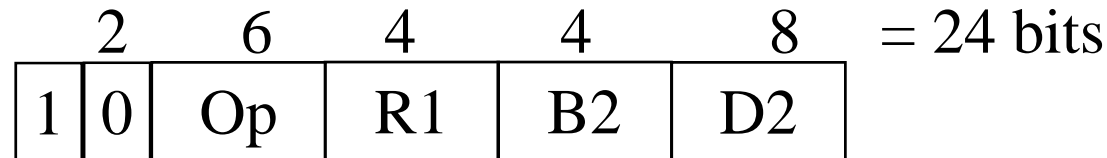
Format A:



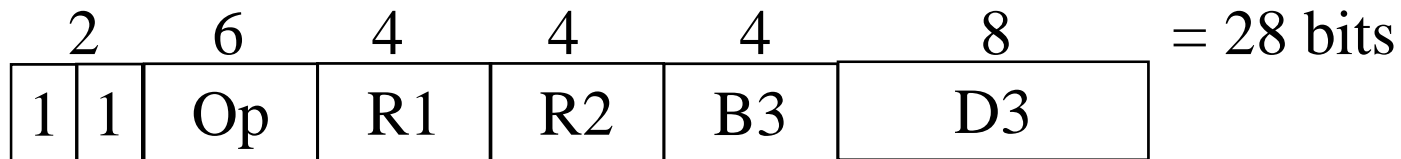
Format B:



Format C:



Format D:



You need to develop an instruction set and formats that support the following operations:

$R1 \leftarrow R1 \text{ OP } R2$, 16 instructions

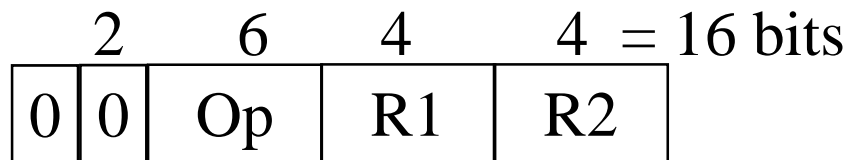
$\text{MEM} \leftarrow R1$, 4 instructions

$R1 \leftarrow R2 \text{ OP } R3$, 32 instructions

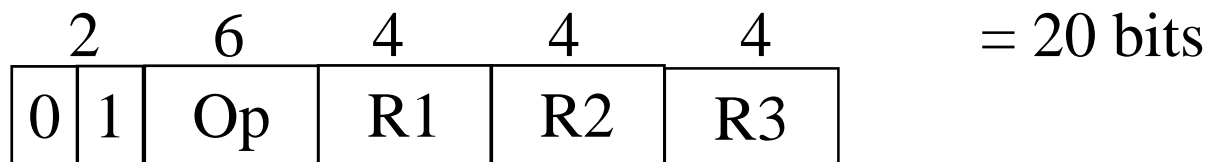
The machine has 8 general purpose registers, each 16 bits in size. Memory is accessed by a base plus displacement of 12 bits.

Go through the analysis and design.

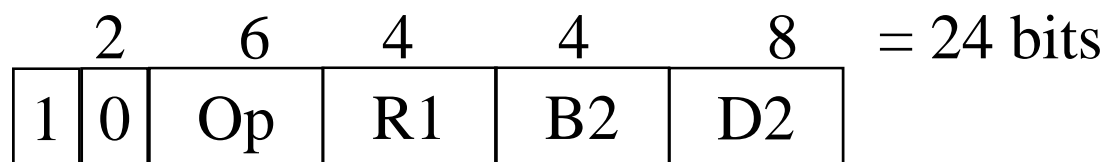
Format A:



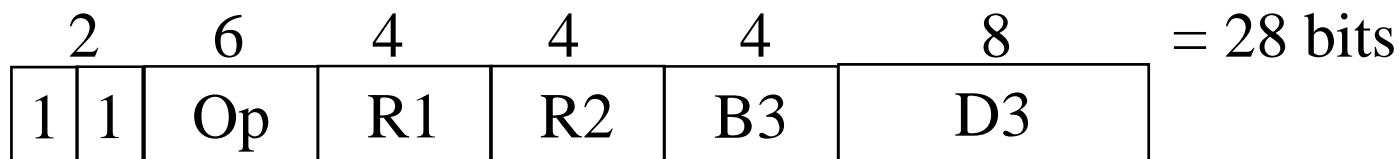
Format B:



Format C:



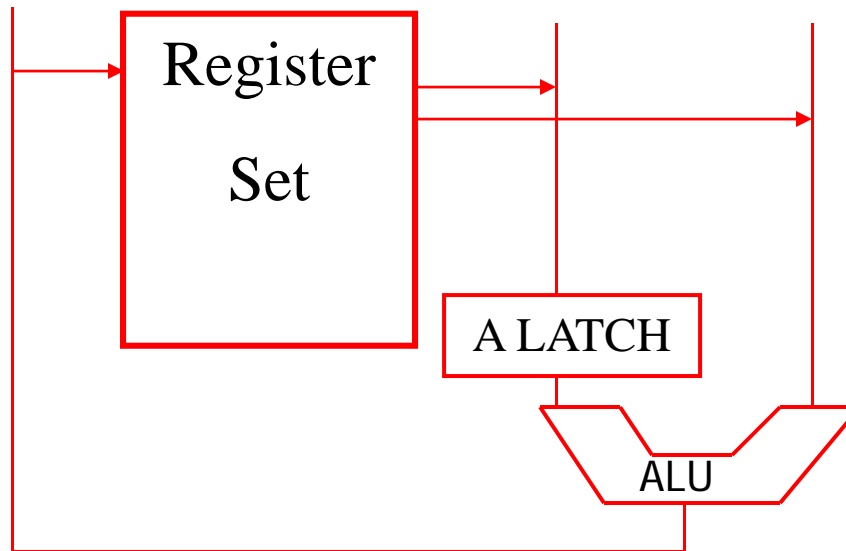
Format D:



From Format A we need:

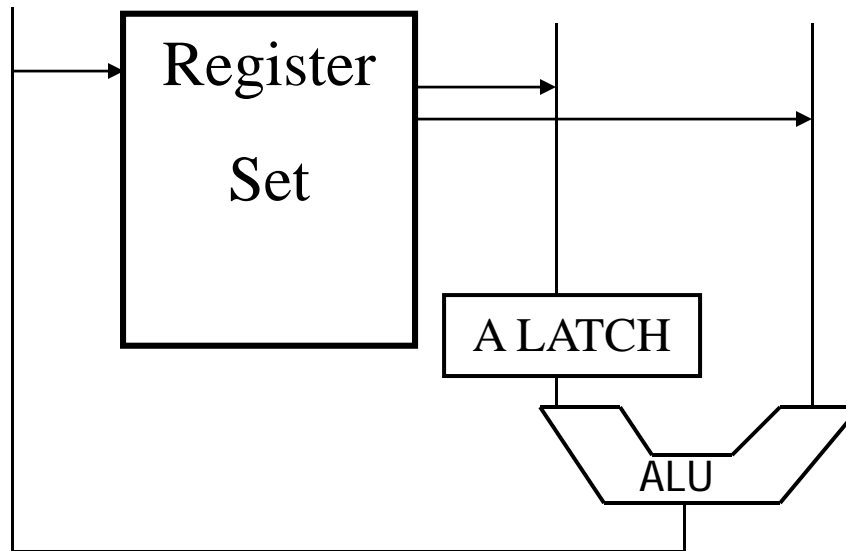
$R1 \leftarrow R1 \text{ OP } R2$

OP R1 R2

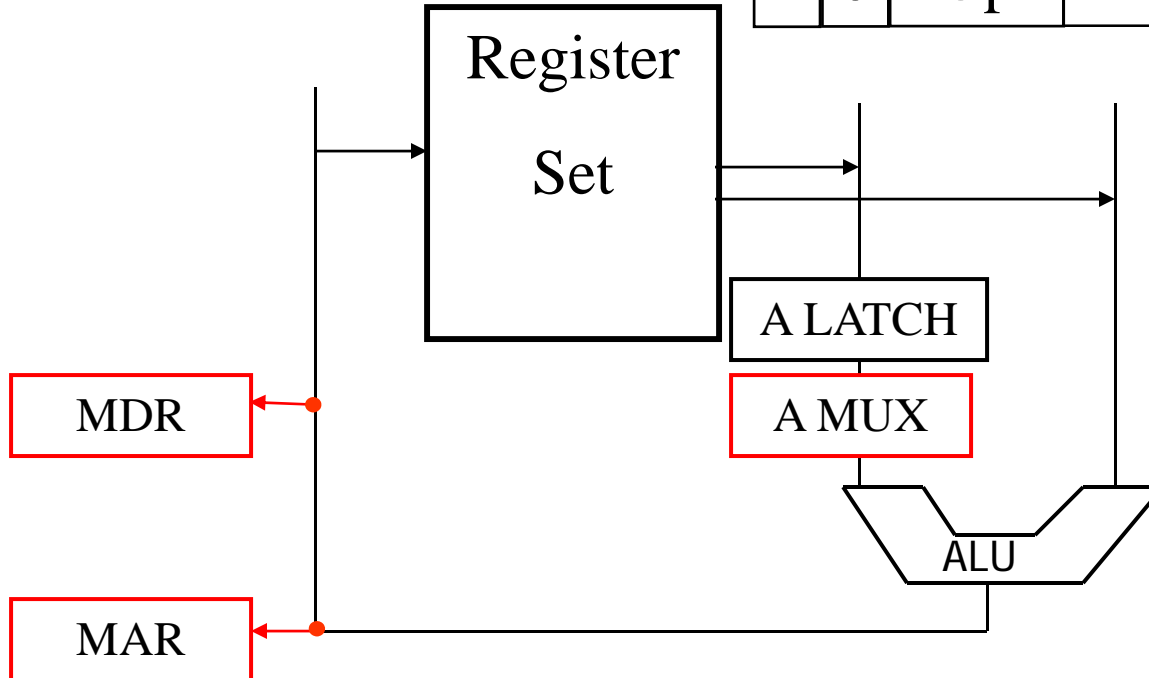
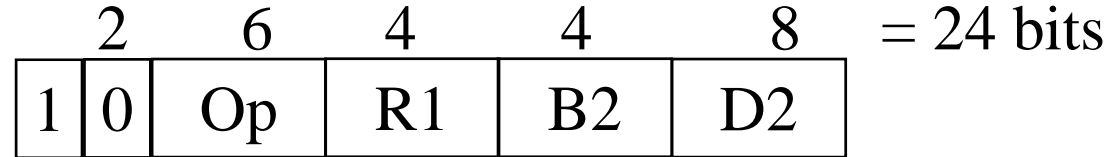


From Format B we Add:

Nothing else needed in terms of pathways



From Format C we Add:



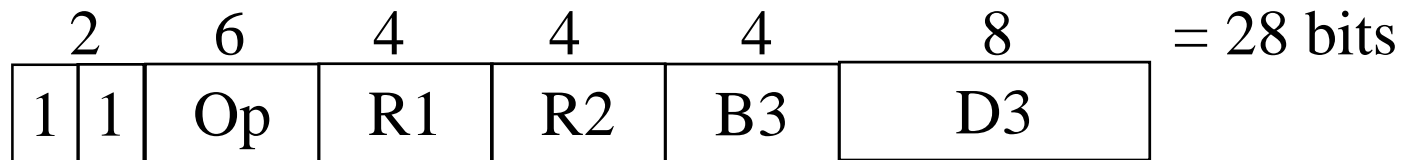
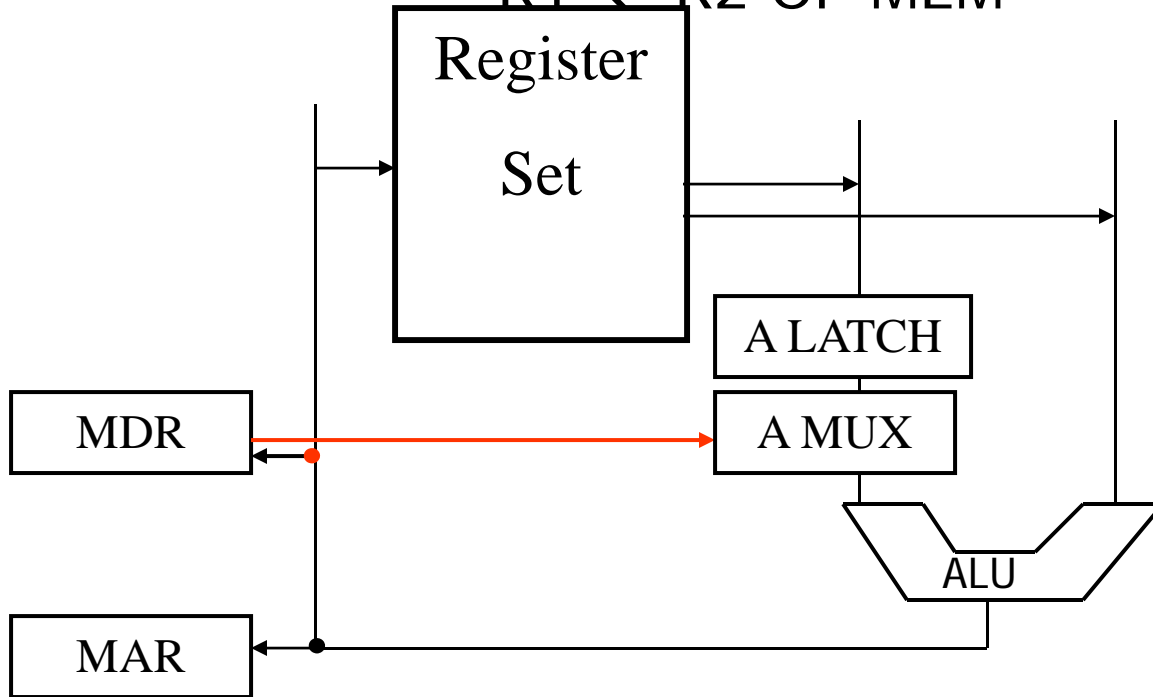
From Format D we Add:

MEM ← R1 OP R2

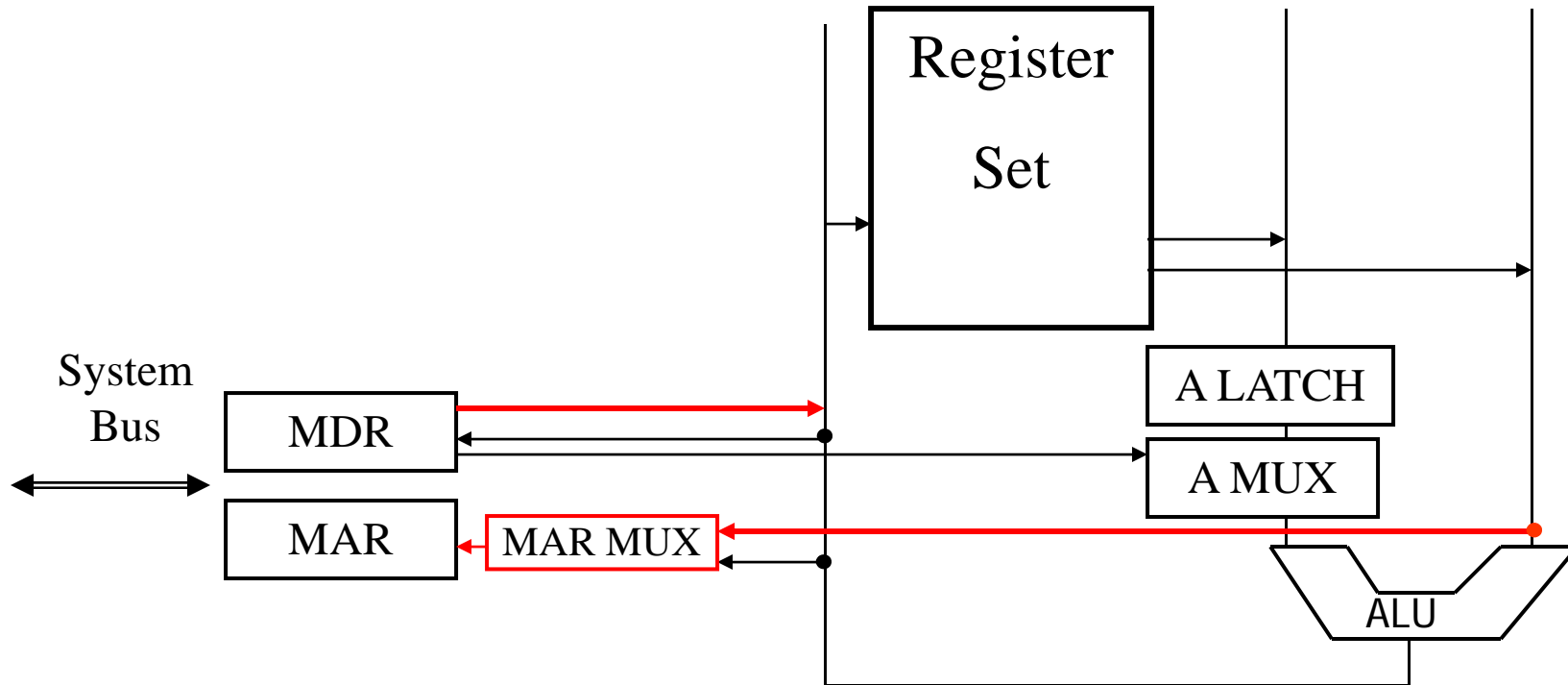
R1 ← R2 OP MEM

OP R1 R2 B3 D3

OP R1 R2 B3 D3



- Address of next instruction is in a register: PC
- Address must be sent to the MAR, AND be incremented and returned to the PC.



**End
Of
Today's
Lecture.**

