L16-CS8421-InstSet-P1
Introduction to Instruction Sets
CS8421
Computing Systems
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Class
Will
Start
Momentarily...
Chapter 10 material in Stallings
Chapter 10 in Concepts in Computing

• Instruction formats
• Classic IBM 370 formats
• Instruction Set Design
• Instruction Set Analysis
• Many computers support more than a single format for instructions
• Computers can support variable size instructions, in terms of bits required
• Relating instruction format size to data bus width:
  – Instructions that are smaller in size than the size of the data bus: 16 bit instruction on a 32 bit bus – multiple instructions in a single fetch!
  – Instructions that are wider than the data bus: requires multiple fetches for the entire instruction
• Instructions sets differ in terms of instruction formats supported.
• Instruction formats primarily differ in terms of the number and type of operands that they work with.

<table>
<thead>
<tr>
<th>Operands</th>
<th>Symbolic Rep</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>OP,A,B,C</td>
<td>A &lt;- B OP C</td>
</tr>
<tr>
<td>2</td>
<td>OP,A,B</td>
<td>A &lt;- A OP B</td>
</tr>
<tr>
<td>1</td>
<td>OP, A</td>
<td>AC &lt;- AC OP A</td>
</tr>
<tr>
<td>0</td>
<td>OP</td>
<td>Top &lt;- Top OP (Top-1)</td>
</tr>
</tbody>
</table>
Types of Instructions

- Data Transfer
  - Move, store, load, push, pop
- Arithmetic
  - Add, Sub, Mult, Div, Inc, Dec, etc.
- Logical or bit operations
  - AND, OR, NOT, XOR, TEST, COMPARE, SHIFT, ROTATE
- Control
  - Jump, branch, branch on, return
- Input/Output
  - INPUT, OUTPUT, START (I/O)
- Data Conversion
  - Convert, convert between formats, binary, BCD, Packed, etc.
• RR Format (Reg to Reg)

\[
\begin{array}{cccc}
2 & 6 & 4 & 4 \\
0 & 0 & \text{Op} & \text{R1} & \text{R2} \\
\end{array}
\]

= 16 bits

R1 \leftarrow R1 \text{ Op} \text{ R2}

R1 and R2 are 4 bits. What does that tell us about the architecture?

Opcode is 6 bits. What does that tell us about this format?

Note: 32-bit registers
• RX Format

\[
\begin{array}{cccccc}
0 & 1 & \text{Op} & R1 & I2 & B2 & D2 \\
\end{array}
\]

\[
\begin{array}{cccccc}
2 & 6 & 4 & 4 & 4 & 12 \\
\end{array}
\]

\[
R1 \leftrightarrow R1 \text{ Op (EA)} \quad \text{Effective Address is:} \quad (B2) + (I2) + D2
\]

Effective Address

D2 is 12 bits. What does that tell us?

Excellent format for working with arrays.
• RS Format - three operand instruction

2  6  4  4  4  12 = 32 bits
1 0  Op  R1  R3  B2  D2

R1 ← R3 Op (EA)    Effective Address is:   (B2) +D2

------------

Effective Address
• **SS Format**, 48 bits!

<table>
<thead>
<tr>
<th></th>
<th>2</th>
<th>6</th>
<th>8</th>
<th>4</th>
<th>12</th>
<th>4</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Op</td>
<td>L</td>
<td>B1</td>
<td>D1</td>
<td>B2</td>
<td>D2</td>
</tr>
</tbody>
</table>

Memory to Memory instruction. Example:
Move L bytes from location 1 to location 2
<table>
<thead>
<tr>
<th>Format</th>
<th>Opcode Byte</th>
<th>Hex Digits</th>
</tr>
</thead>
<tbody>
<tr>
<td>RR</td>
<td>00XX XXXX</td>
<td>0-3 0-F</td>
</tr>
<tr>
<td>RX</td>
<td>01XX XXXX</td>
<td>4-7 0-F</td>
</tr>
<tr>
<td>RS</td>
<td>10XX XXXX</td>
<td>8-B 0-F</td>
</tr>
<tr>
<td>SS</td>
<td>11XX XXXX</td>
<td>C-F 0-F</td>
</tr>
</tbody>
</table>

If ADD=001000 and SUB=000100, then what is (in hex):
04B3

8834CBF0
Design instruction formats for an instruction set with only the following two types of instructions:

Format A:  Reg,Reg:  \( R1 \leftarrow R1 \text{ OP } R2 \)
Format B:  Reg,Mem  \( R1 \leftarrow R1 \text{ OP Mem} \)

The machine has 16 registers.
There are 32 instructions of type A.
There are 16 instructions of type B.
Memory access is a displacement of 13 bits plus a base register.
Format A:

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>R1</th>
<th>R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Op</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

\[ \text{1 5 4 4 = 14 bits} \]

Format B:

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Op</td>
<td>R1</td>
<td>B2</td>
<td>D2</td>
</tr>
</tbody>
</table>

\[ \text{1 4 4 4 13 = 26 bits} \]
Design instruction formats for an instruction set with only the following three types of instructions:

Format A: Reg,Reg: R1 ← R1 OP R2
Format B: Reg,Mem R1 ← R1 OP Mem
Format C: Reg,Reg,Mem R1 ← R2 OP Mem

The machine has 32 registers.
There are 4 instructions of type A.
There are 8 instructions of type B.
There are 16 instructions of type C.
Memory access is a displacement of 8 bits plus a base register.
End

Of

Today’s

Lecture.