L09-CS8421-9-17-2008

Chapter 3: Interrupts & Interconnects

CS8421
Computing Systems
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Class
Will
Start
Momentarily…

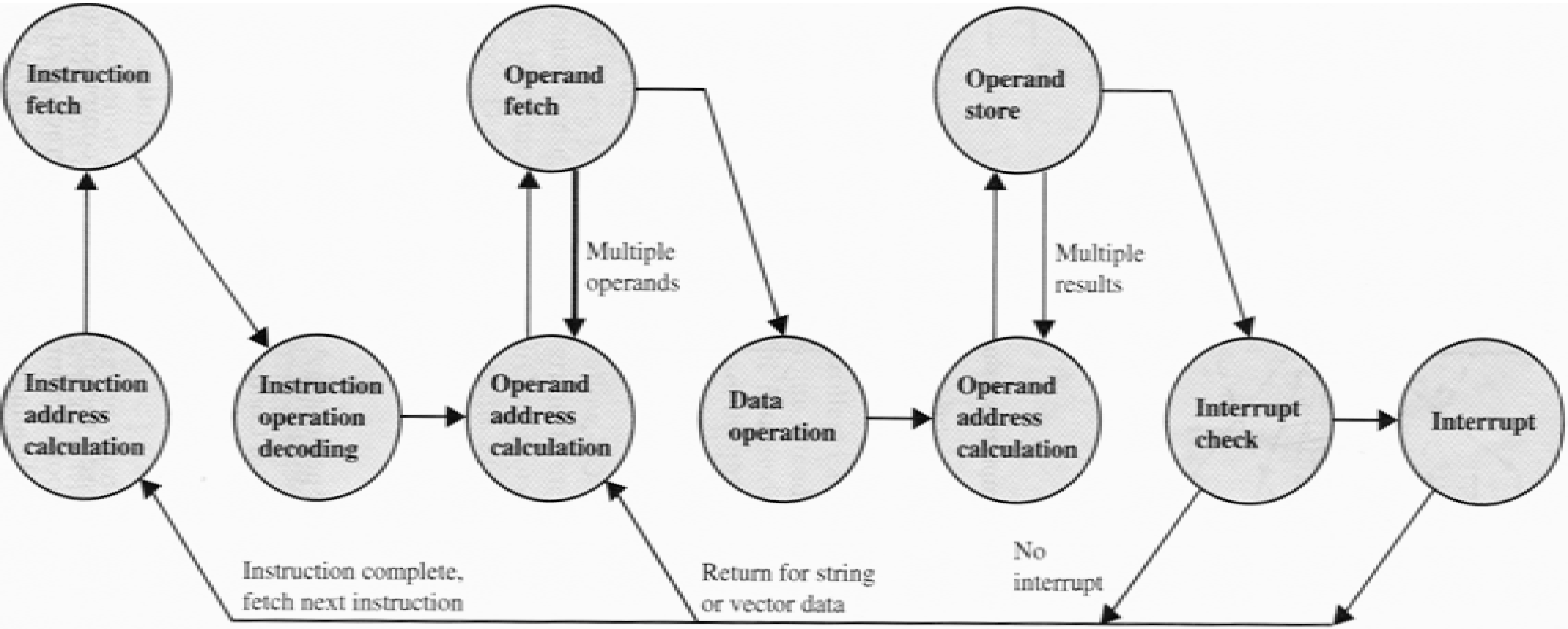
Monday, Sept 9

- Homework problem
- Topics from Chapter 3, Stallings:
  - Interrupts
  - Interrupts and efficiency
  - Instruction Cycle Diagram w Interupts
  - Computer Architecture – the Interconnection Network & Topology
  - Clustered Architecture
  - Bus Arbitration
  - Synchronous Bus Operations

Homework

300	1940
301	5941
302	2941
303	3942
304	2943
940	0003
941	0005
942	0004
943	0001

Fetch/Decode/Execute/Interrupt Cycle

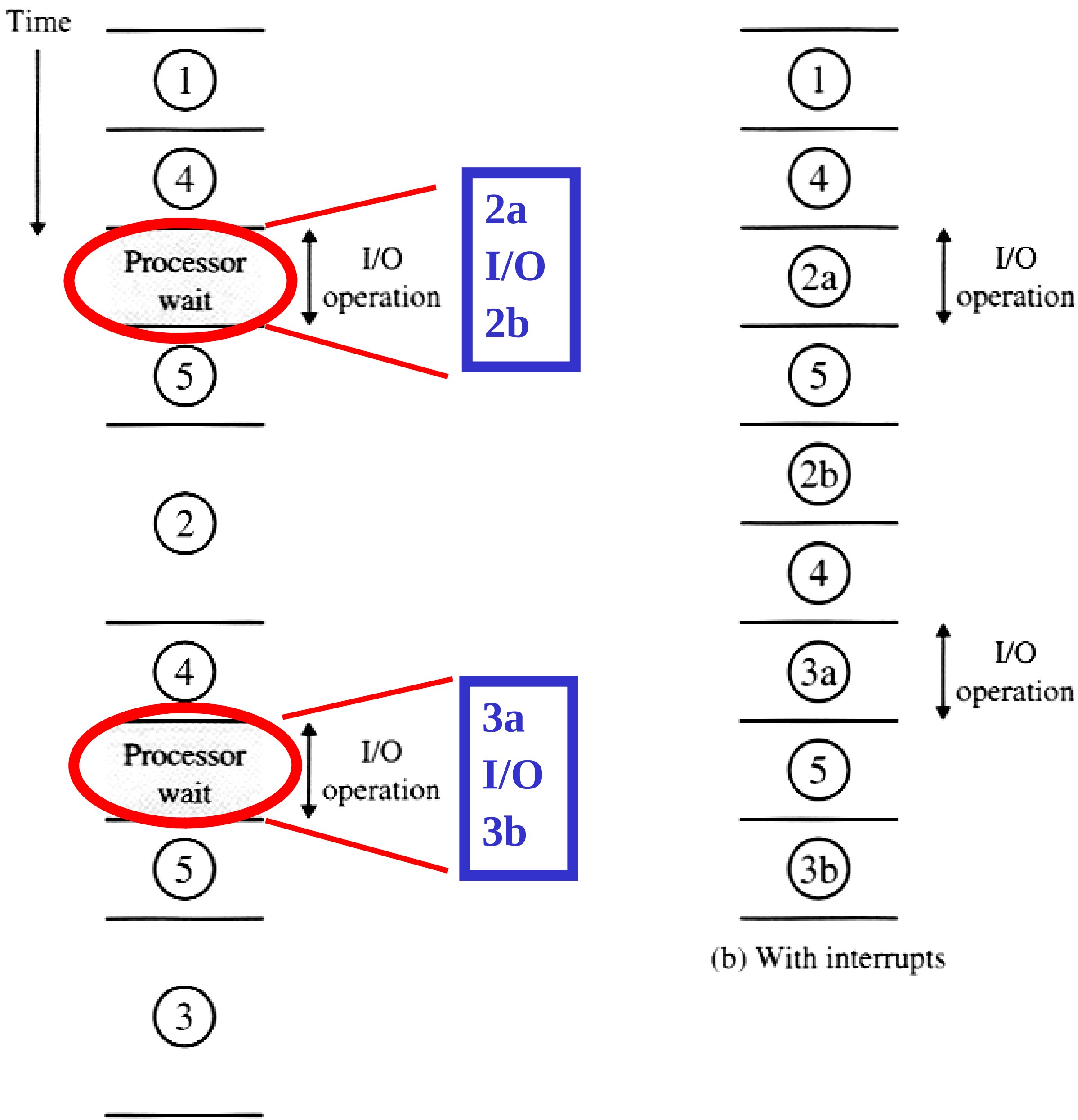


Interrupt Servicing

- Servicing an Interrupt

1. Save the current state of processing (push registers onto a data structure called a stack)
2. Use the interrupt as an index into a table of Interrupt Service Routines
3. Jump to the ISR identified by the interrupt
4. Complete the ISR
5. Restore the state: “pop” the saved values from the stack, back to the registers
6. Continue processing

Interrupts and Processor Utilization



(b) With interrupts

2a & 2b are the ISR code that the processor must complete. Then, the device can work on its own when using interrupts.

A form of parallel of concurrent processing.

Interruptable Interrupts

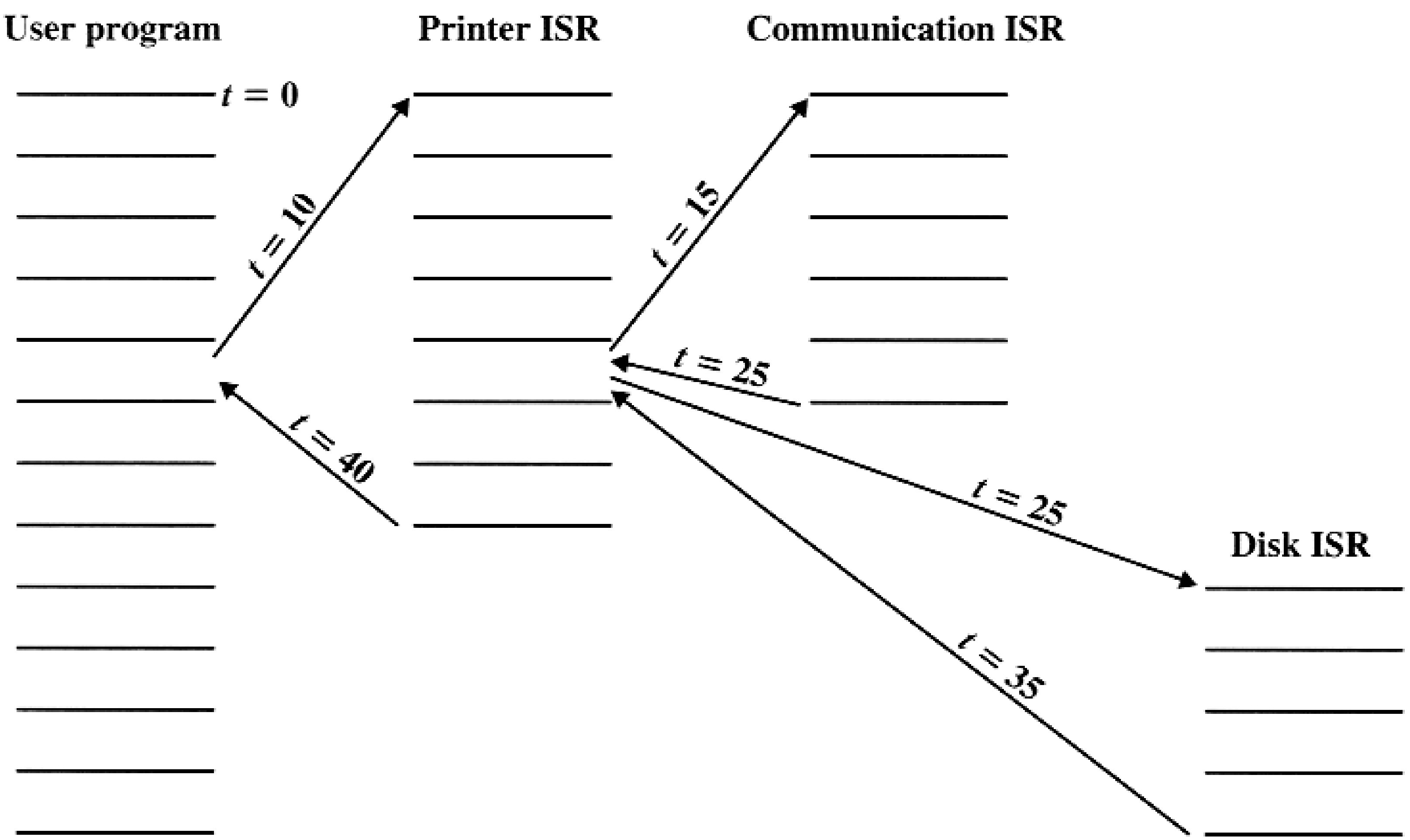
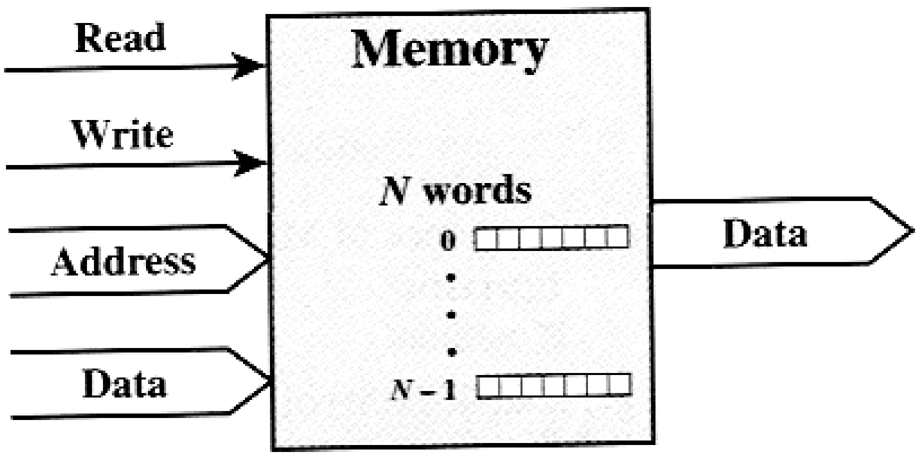
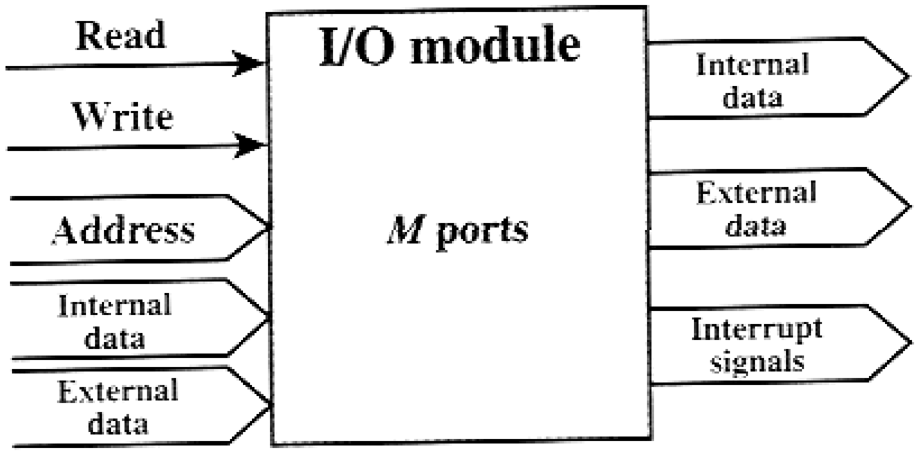
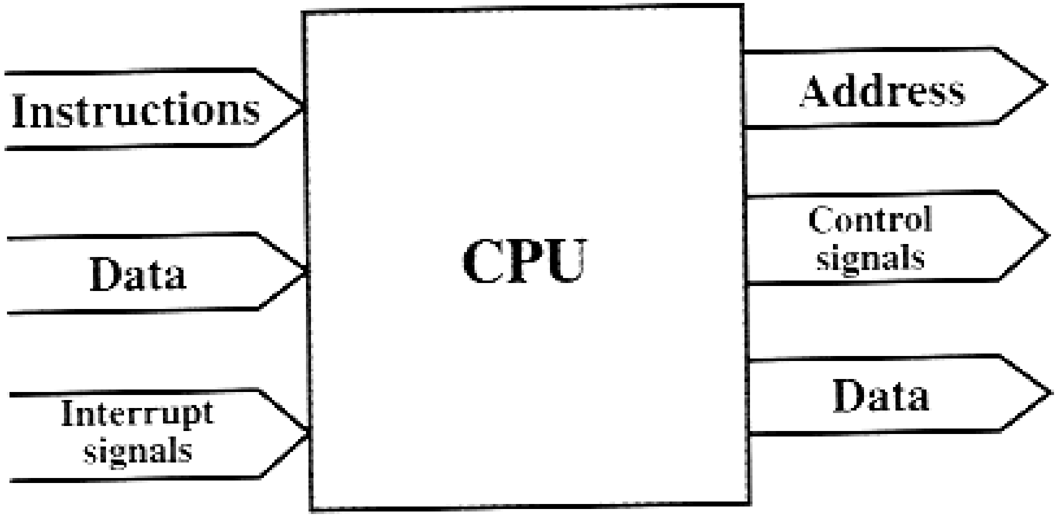


Figure 3.14 Example Time Sequence of Multiple Interrupts [TANE90]

Component Communication







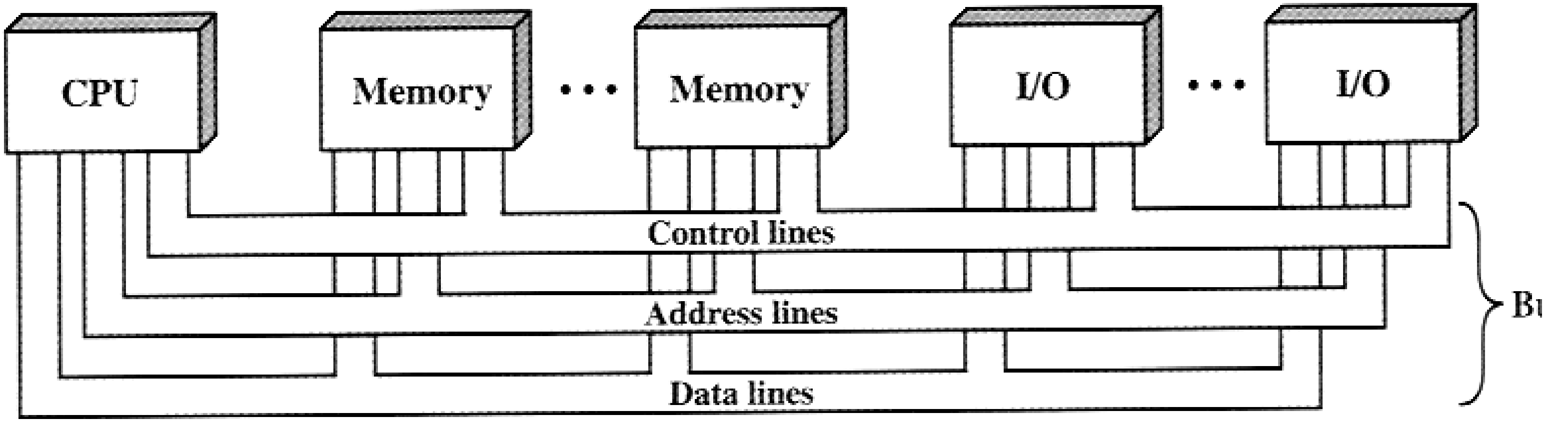
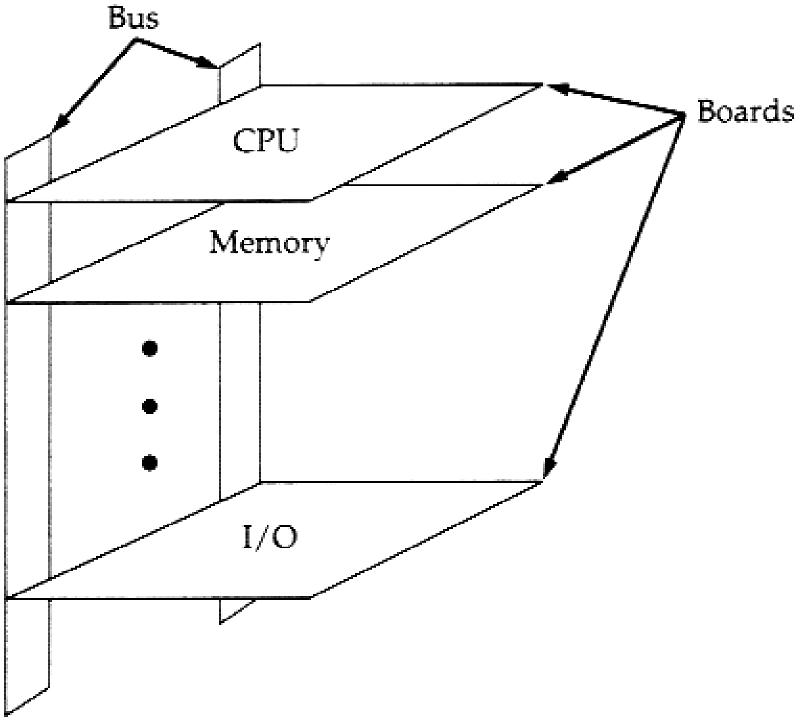


Figure 3.16 Bus Interconnection Scheme

Note: 3 types of bus lines

- •Control
- •Address
- •Data

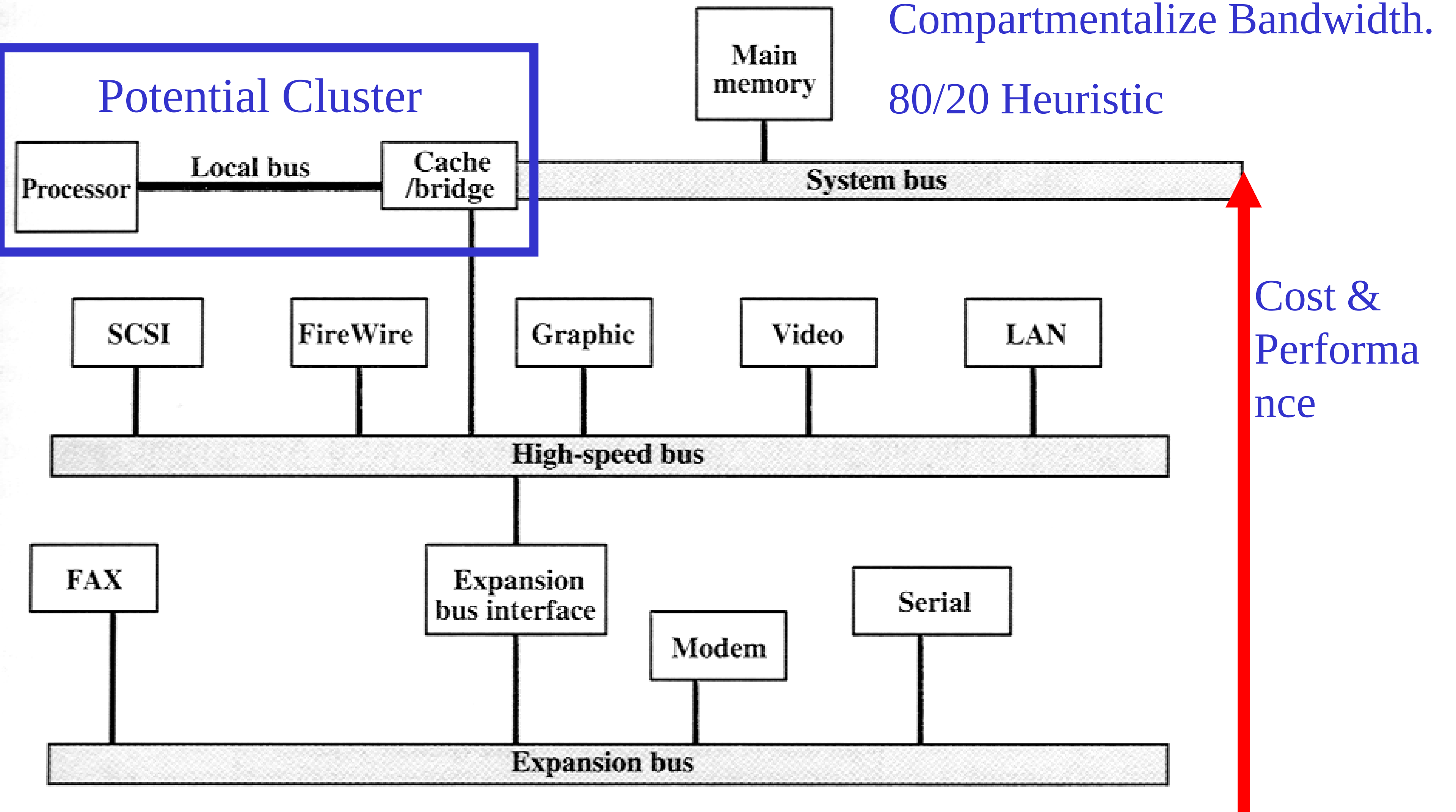
Back-plane Construction



Multi-Bus Architecture

Compartmentalize Bandwidth.

80/20 Heuristic



(b) High-performance architecture

Bus Arbitration

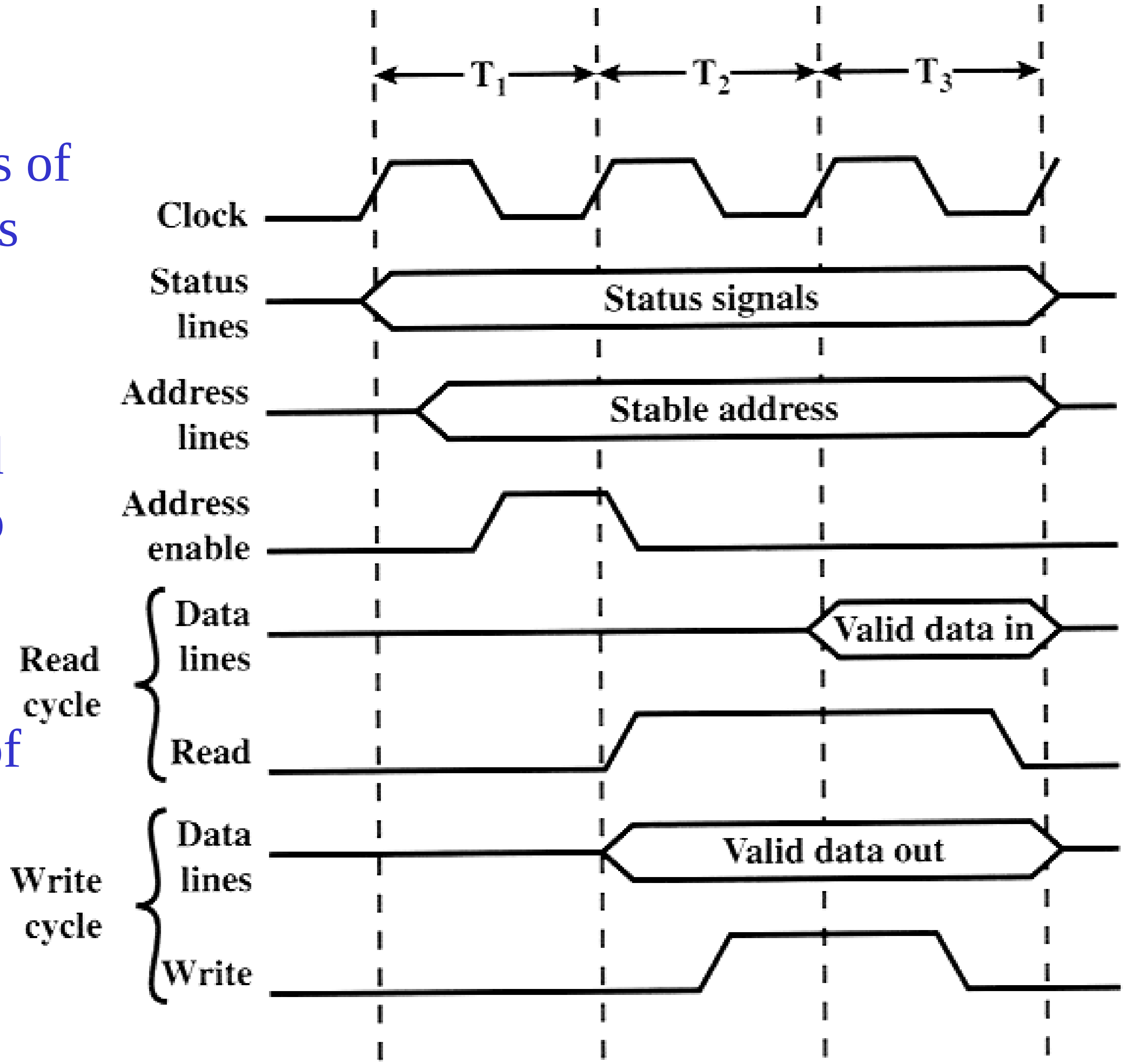
- Shared Bus – How to "take turns" or resolve conflicts
- Contention – multiple devices compete for a limited resource. Devices contend for access to the bus.
- Resolve contention:
  - Priority (unfair)
  - "Round-Robin" take turns in specific order
  - A "protocol" implemented in logic (ethernet is an example)
- May use an "arbiter", a device or chip that includes the logic or protocols used to resolve contention
  - More details later, as time allows

Synchronous Bus Timing

A standard – design specifications in terms of timing. Many vendors can build to specifications.

Devices must respond within timing specs to work.

Faster devices will be limited by the speed of the bus.



End of Lecture

End

Of

Today's

Lecture.

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